METHOD AND APPARATUS FOR GENERATING A SEQUENCE OF CLOCK SIGNALS

ABSTRACT OF THE DISCLOSURE

A clock generator circuit generates a sequence of clock signals equally phased from each other from a master clock signal. The clock generator is formed by inner and outer delay-locked loops. The inner delay-locked loop includes a voltage controlled delay line that delays a reference clock applied to its input by a plurality of respective delays. Two of the clock signals in the sequence are applied to a phase detector so that the signals at the outputs of the delay line have predetermined phases relative to each other. The outer delay-locked loop is formed by a voltage controlled delay circuit that delays the command clock by a voltage controlled delay to provide the reference clock to the delay line of the inner delay-locked loop. The outer delay-locked loop also includes a phase detector that compares the command clock to one of the clock signals in the sequence generated by the delay line. The outer delay-locked loop thus locks one of the clock signals in the sequence to the command clock. As a result, all of the clock signals in the sequence generated by the delay line have respective predetermined phases relative to the phase of the command clock. One of the clock signals in the sequence is selected by a multiplexer to clock a command data latch at a time corresponding to the delay in coupling a command data bit to the latch.